REMARKS

An Office Action was mailed February 6, 2009. This Response is timely. Any fee due with this paper, including any necessary extension fees, may be charged on Deposit Account 50-1290.

An interview was conducted on May 29. Agreement on the claims was not reached. Nonetheless, the Examiner is thanked for courtesies and considerations extended.

Summary

Claims 1-3, 5, and 11-18 are being examined. Claim 1 is the only independent claim.

By the foregoing, claim 1 is amended, claim 16 is cancelled, and new claims 19-26 including new independent claims 19 and 26, are presented. No new matter has been added. All new claims are directed to subject matter being examined in the application.

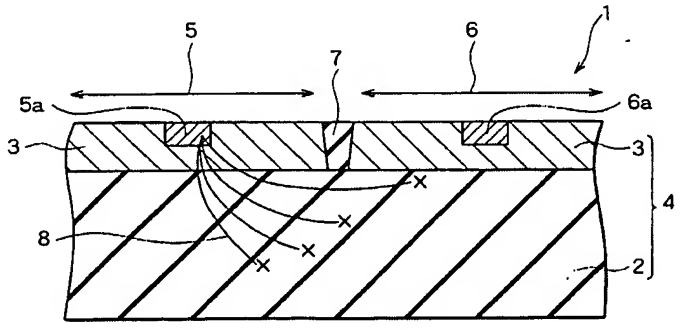
Rejections in view of Williams

Claims 1, 5, 11-13, 16, and 18 stand rejected under 35 U.S.C. §102(b) as being anticipated by or stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,156,989 to Williams.

Claims 1 and 19 recite

> *[a] device isolation region is spaced apart from the first and second circuit by respective portions of the silicon epitaxial layer.*

Support thereof may be found, inter alia, at 10:27 and Fig. 3.



The presently claimed invention comprises first and second circuits comparable to the DMOS structures of Williams.

In contrast, Williams does not teach, disclose, or suggest the claimed invention. Williams teaches an isolation region 125, 129a, 141a, 141b, 165, and 167. 9:66 et al, Fig. 25P. As seen in Fig. 25P, Williams also teaches that the DMOS structures are in contact with the device isolation region.

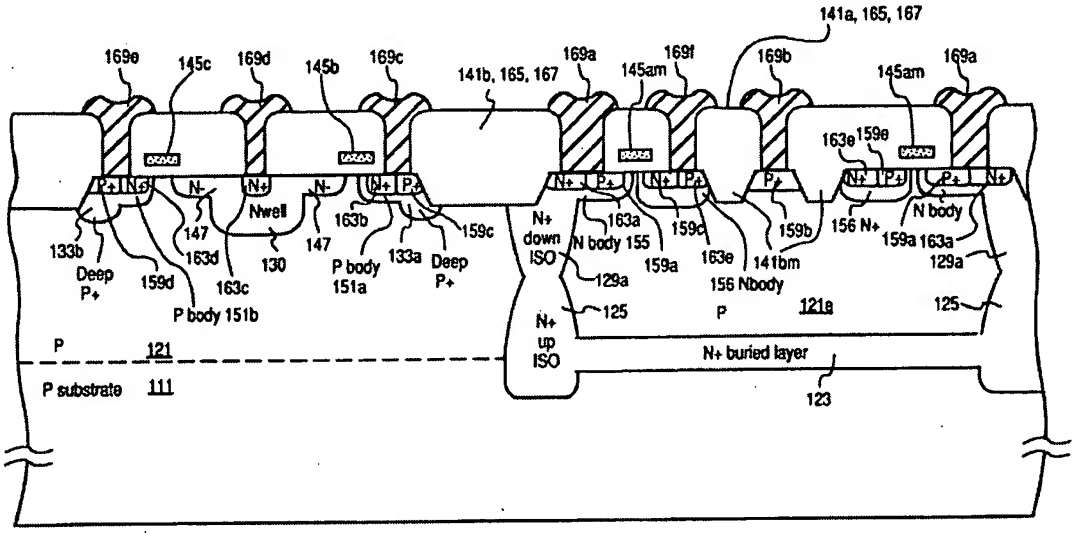


Fig. 25P

Indeed, the presently claimed invention is not obvious over Williams since it includes unpredictable results when the device isolation region is spaced apart from the first and second circuit sections.

As is generally known in the art, an interface state is formed at an interface between the device isolation region and the silicon epitaxial layer. When the device isolation region is made of silicon oxide, the interface state has a density of 1E10 cm^{-2} to 1E12 cm^{-2}. At the interface state, an electron or a hole is captured or emitted, and thereby transmitts the electric signal including electric noise at the interface.

As is also generally known in the art, a response speed for capturing or emission of an electron or a hole in the interface state is relatively slow compared to ordinary electric signal frequencies.

Thus, the electric signal is not affected by the stray electron since it is not suitably transmitted at the interface. However, a low frequency noise, for example, a switching noise, is transmitted at the interface using the interface state.

When the first and second circuits contact the device isolation region, the first and second circuits are in contact with the interface between the silicon epitaxial layer and the device isolation region. This causes the transmission of the noise between the first and second circuits via the interface.

Therefore, in the presently claimed invention, by spacing the device isolation region apart from the first and second circuits, the integrated circuit can effectively suppress the transmission of the noise. This unexpected result is not taught, disclosed, or suggested in the cited references.

Thus, the claimed structure is not taught by Williams. Accordingly, the Examiner is respectfully requested to withdraw the rejection.

Rejections in view of Crichi

Claims 1, 12, and 13 stand rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,559,349 to Crichi. Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Crichi.

Independent claims 1 and 19 recite

> *[a] device isolation region is spaced apart from the first and second circuit by respective portions of the epitaxial layer.*

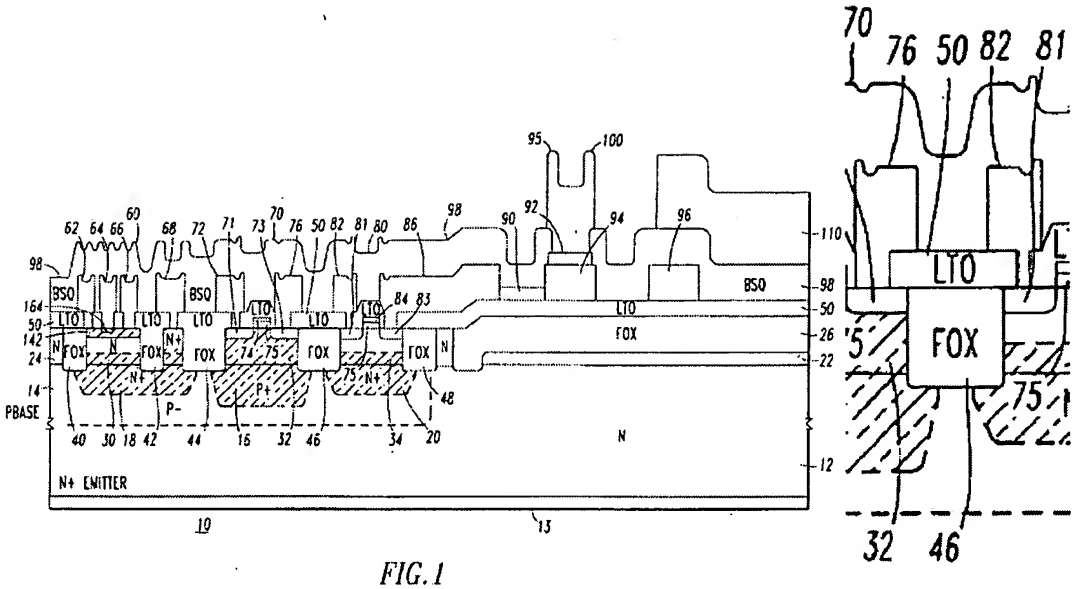


FIG. 1

Recessed field oxide area (FOX) 46 is cited as the device isolation region and which abut, presumably, positive drain region 73 and, presumably, negative drain region 81 - neither is mentioned in the specification, but see 4:60 et al. As is evident, the FOX layer rather than being spaced apart from the first and second circuit by respective portions of the epitaxial layer is in direct contact with the drain regions of the circuit.

Accordingly, the Examiner is respectfully requested to withdraw the rejection.

Rejections in view of Williams and Crichi

Claims 2, 3, and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Williams in view of Crichi.

As discussed above, Crichi and Williams both lack the essential teachings related to one or the other teachings. Thus, one could not fill the gaps of the other.

Claim 14 recites

> *a first impurity concentration of the p-type bulk substrate is one-hundredth or less a second impurity concentration of the p-type bulk epitaxial layer*

Thus, claim 14 recites a unique impurity density. This impurity density is in inverse proportion to the resistivity. As taught by the Applicant in Fig. 4, in the presently claimed invention the substrate resistivity dramatically decreases the noise transmission when changing 10 Ohm-cm to 1000 Ohm-cm of the substrate resistivity. Thus, as taught in 13:7-17, by inhibiting the noise transmission to a practically sufficient level, the numerical limitation recited in claim 14 of the present application is achieved.

The combination of William or Crichi, or each of these references alone, teach, disclose, or suggest this inventive structure. Accordingly, the Examiner is respectfully requested to withdraw the rejection.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Respectfully submitted,

/Hassan A. Shakir/
Hassan A. Shakir
Reg. No. 53.922
212.940.6489

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